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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,050	09/30/2003	Zenko Gergintschew	WMP-IFT-823	5870

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,050	GERGINTSCHEW, ZENKO	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Balakrishnan et al., Patent No. 6,781,357. With respect to claim 1, applicant's prior art [Fig. 1 and Fig. 2A] teaches a method for driving a semiconductor switch and circuit configuration with a semiconductor switch. A method comprises a semiconductor switch [Fig. 1, T] having load current limiting [Fig. 1, Current Sensor 2] and thermal protection [Fig. 1, Temperature Sensor 1), the semiconductor switch [Fig. 1, T] switching off upon a predetermined upper temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tso] being exceeded and switching on again when a chip temperature falls below a predetermined lower temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tsu] as disclosed in applicant's specifications page 11, lines 18-26 and Fig. 2A; operating the semiconductor switch in one of a normal mode [Fig. 1, The semiconductor switch T is in a normal mode when the chip temperature falls below a given lower chip temperature, or when the switch T is on] and a fault mode [Fig. 1, The semiconductor switch T is in a fault mode when the chip temperature exceeds an upper temperature value, or when the

switch T is off]; operating the semiconductor switch in the fault mode upon exceeding the predetermined upper temperature [Fig. 2A, Refer to the graph of Chip Temperature Ts, Tso] as disclosed in applicant's specifications, page 11, lines 18-20.

However, the prior art fails to teach or suggest limiting a load current to a first maximum value in the normal mode and to a second maximum value, being lower than the first maximum value, in the fault mode.

Balakrishnan teaches a power supply including a regulation circuit that maintains an approximately constant load current with line voltage. Balakrishnan teaches limiting a load current [regulating, Abstract, lines 1-2] to a first maximum value [Abstract, lines 1-8, Col. 1, lines 44-52, The first upper level is the upper threshold of normal mode range] in the normal mode and to a second maximum value [The second lower level is below the threshold of normal mode range, which is below the upper threshold], being lower than the first maximum value, in the fault mode [Outside of normal mode range, Col. 1, lines 44-52].

Both teachings are related by both being semiconductor switches having a current limiter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Balakrishnan et al., which teaches a regulation circuit current limit threshold having two levels of thresholds, into the method of the applicant's acknowledged prior art because a rise in current normally accompanies rise in temperature. In normal mode, the load current should be measured and should not exceed a

threshold value. In cases of overload conditions, a rapid increase in current normally accompanies a rapid increase in temperature.

With respect to claim 2, applicant's prior art teaches that the method further comprises switching on the semiconductor switch T when the chip temperature falls below the predetermined lower temperature Tsu in the normal mode and in the fault mode as disclosed in specifications page 11, lines 18-26 and Fig. 2A.

With respect to claim 3, applicant's prior art teaches that the method further comprises switching off the semiconductor switch T, when in the fault mode, if a further upper temperature Tsu is exceeded, the further upper temperature Tsu is lower than the predetermined upper temperature Tso.

With respect to claim 4, Balakrishnan et al. teaches that the method further comprises limiting the load current by actuating the semiconductor switch 2 as disclosed in Col. 1, lines 50-52 and Fig. 1.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Balakrishnan et al., Patent No. 6,781,357 and Thomas, Patent No. 6,052,268. Applicant's acknowledged prior art and Balakrishnan et al. do not teach that the method further comprises monitoring a voltage across a load path of the semiconductor switch; and operating the semiconductor switch in the normal when a load path voltage is smaller than a predetermined threshold value.

Thomas teaches an electrical apparatus which comprises a semiconductor-switching device 3 and a voltage sensing device 5 to monitor a voltage across a load path of the semiconductor switch 3 as disclosed in Col. 2, lines 30-33 and Fig. 1.

All three teachings are related by being semiconductor switches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to combine the teachings of Thomas, which teaches a method of calculating power dissipation through a semiconductor switch using voltage and current sensors, along with the applicant's acknowledged prior art because during overload conditions, current flow along with power dissipation increases dramatically through a transistor. Taken together, Thomas's method of measuring power dissipation can be combined with the method of switching between two operating levels to produce the applicant's method of detecting overvoltage, to more accurately measure current flow.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Brown, Patent No. 5,757,203. With respect to claim 6, applicant's prior art [Fig. 1] teaches a method for driving a semiconductor switch and circuit configuration with a semiconductor switch. A circuit configuration [Fig. 1] comprises a semiconductor switch [Fig. 1, T] having a drive terminal [Fig. 1, Gate electrode of the semiconductor switch T] and a load path [Fig. 1, Path between the semiconductor switch T and Load]; a protective circuit [Fig. 1, Protective Circuit] connected to the drive terminal [Fig. 1, Gate

electrode of the semiconductor switch T] of the semiconductor switch [Fig. 1, T]; a temperature sensor [Fig. 1, Temperature Sensor, 1] disposed in a region of the semiconductor switch [Fig. 1, T, The temperature sensor is disposed near semiconductor switch] and coupled to the protective circuit [Fig. 1, Protective Circuit], the temperature sensor [Fig. 1, 1] providing a temperature measuring signal [Fig. 1, TS] fed to the protective circuit [Fig. 1, Protective Circuit]; and a current measuring configuration [Fig. 1, Current Sensor, 2] coupled to the protective circuit [Fig. 1, Protective Circuit] and generating a current measuring signal [Fig. 1, IS] being dependent on a current across the load path of the semiconductor switch [Fig. 1, T].

However, the prior art fails to teach or suggest a protective circuit storing first and second overcurrent signals, and protective circuit assuming one of a first operating mode and a second operating mode, and, depending on a mode, said protective circuit controlling the semiconductor switch.

Brown teaches multiple on-chip IDDQ monitors to excess leakage current detection for integrated circuits which can be used for determination of defective integrated circuits. Brown teaches a storage element storing first overcurrent signal and second overcurrent signal as disclosed in Col. 7, lines 40-41.

Both teachings are related by being current sensors for the IC circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brown, which teaches a storage element storing first and second overcurrent signals, along with the

applicant's acknowledged prior art to measure IDDQ defect in the presence of much larger normal quiescent current without substantially adding to the size of the IC die. Taken together, Brown's method of storing first and second overcurrent signals can be easily combined with the method of switching between two operating levels to produce the applicant's method of detecting overcurrent, to more accurately measure current flow.

Allowable Subject Matter

4. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: With respect to claim 7, applicant's acknowledged prior art (Fig. 1) teaches a method for driving a semiconductor switch and circuit configuration with a semiconductor switch, but does not teach a protective circuit storing first and second overtemperature signals, and, depending on the mode, said protective circuit drives said semiconductor switch into a blocking state according to a comparison of the temperature measuring signal to the first overtemperature signal or according to a comparison of the temperature measuring signal to the second overtemperature signal. This is not anticipated or rendered obvious by the prior art reference.

With respect to claim 8, applicant's acknowledged prior art (Fig. 1) teaches a method for driving a semiconductor switch and circuit configuration

with a semiconductor switch, but does not disclose a voltage measuring configuration for detecting a load path voltage of said semiconductor switch and connected to said protective circuit, said voltage measuring configuration providing a voltage measuring signal that is fed to said protective circuit, said protective circuit assumes one of the first and second modes depending on the voltage measuring signal. This is not anticipated or rendered obvious by the prior art reference.

Response to Arguments

5. Applicant's arguments filed on 03/17/2006 have been fully considered but they are not persuasive.

With respect to the arguments on the last paragraphs of page 5 and page 6, Balakrishnan implicitly protects against over temperature because his regulation circuit is designed to keep the current in a normal operating range. Since restricting current to an upper and a lower threshold will obviously restrict temperature, the regulation circuit is also effectively temperature-regulating circuit.

With respect to the arguments on the second paragraph of page 6, the applicant's prior art [Fig. 2A] teaches operating the semiconductor switch in one of a normal mode [Fig. 1, The semiconductor switch T is in a normal mode when the chip temperature falls below a given lower chip temperature, or when the switch T is on] and a fault mode [Fig. 1, The semiconductor switch T is in a fault

mode when the chip temperature exceeds an upper temperature value, or when the switch T is off].

With respect to the arguments on the third paragraph of page 7 (lines 4-7), Brown implicitly protects against over temperature because his current detection circuit is designed to keep the current in a normal operating range. Since restricting current obviously restricts temperature, the current detection circuit is also effectively temperature-regulating circuit.

With respect to the arguments on the third paragraph of page 7)lines 8-14), applicant's acknowledged prior art [Fig. 1] teaches a semiconductor switch [Fig. 1, T] which is in a normal mode when switched on [Fig. 1, The semiconductor switch T is in a normal mode when the chip temperature falls below a given lower chip temperature, or when the switch T is on] and is in a fault mode when switched off [Fig. 1, The semiconductor switch T is in a fault mode when the chip temperature exceeds an upper temperature value, or when the switch T is off] as well as a temperature sensor [Fig. 1, Temperature Sensor, 1] disposed in a region of a semiconductor switch and coupled to the protective circuit [Fig. 1, Protective Circuit], the temperature sensor providing a temperature measuring signal [Fig. 1, TS] fed to the protective circuit as recited in claim 6.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
06/10/2006

Stephen W Jackson

6-12-06

STEPHEN W. JACKSON
PRIMARY EXAMINER